Logan Burns

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Education

University of Florida, B.S. Electrical Engineering Expected May 2028
Herbert Wertheim College of Engineering, GPA 3.91, University Honors Program *Gainesville, FL*

- Relevant coursework: Digital Design, Microprocessor Applications, Electronic Circuits, Signals & Systems, Circuits I/II.

Experience

Head Peer Instructor, EEL 3701C Digital Logic & EEL 4744C μP Applications Spr 2026 – Present
Leads the peer-instructor team for both courses, UF ECE *Gainesville, FL*

- Manage exam-grading assignments across the PI team, course hardware inventory, and hardware-repair coordination; point of contact for fellow peer instructors.
- Lead help sessions on external-bus memory mapping, address decoding, and digital logic design; author lab specifications, solutions, and course documentation.
- Resolved a Quartus–Questa incompatibility with a C++ command-line shim distributed to students to restore local HDL simulation; built a JTAG batch-programming and QC pipeline for the course's DE10-Lite FPGA fleet.
- Brought 150 course documents into ADA/WCAG compliance with a custom Python toolchain (contrast analysis, document/PDF tagging, GUI, packaged executable); automated Canvas grade entry with a verified-diff Selenium tool.

Florida Optics and Computational Sensor (FOCUS) Lab, UF ECE Sep 2025 – Present
Undergraduate Research Assistant, embedded systems & thermal instrumentation *Gainesville, FL*

- Built a calibrated FLIR A6751sc thermal-imaging pipeline (GigE Vision) and a 150 W radiant-heat stress rig to characterize ML workloads on a Jetson Orin NX; work contributed to a co-authored conference submission (CoRL 2026), including validation of a controller achieving 16.3 ℃ lower peak temperature at equal accuracy.
- Sole author of a virtual thermal sensing system predicting temperatures of off-die board components (VRMs, MOSFETs) from on-die telemetry: thermal response mapping, lumped-capacitance model fitting, and a real-time Linux daemon (under 1% CPU) needing no camera after a one-time calibration.

Machine Intelligence Laboratory (MIL), UF: SubjuGator 9 AUV Jan 2026 – May 2026
Electrical Team, sole owner of the leak-detection subsystem *Gainesville, FL*

- Designed the vehicle's water-ingress detection board end to end: LTspice comparator front-end simulation, Altium schematic capture and 2-layer layout, and a fabrication-released design (v2) with full manufacturing outputs (gerbers, NC drill, BOM, pick-and-place).

Projects

Polyphonic Wavetable Synthesizer, bare-metal AVR (C, assembly)

- Real-time 3-voice synthesizer on an XMEGA (20 kHz, 12-bit DAC): gapless audio via ping-pong DMA, inline-assembly fixed-point mixing, voice-stealing allocation, per-voice ADSR/filtering, and a live serial oscilloscope display at 2 Mbaud.

Discrete LDO Voltage Regulator, LTspice (individual design)

- Designed and stabilized a discrete LDO: 34 dB worst-case PSRR, phase margin recovered from 2° to 60° via output-capacitor ESR zero placement, and foldback current limiting cutting worst-case pass-FET dissipation from 9.3 W to 2 W.

FPGA Digital Design & Verification, VHDL/SystemVerilog (DE10-Lite)

- Built a complete 2-player Pong entirely in hardware (11-module VHDL design with reusable VGA subsystem); verified designs with constrained-random testbenches, functional coverage, and SystemVerilog Assertions in QuestaSim.

Fabrication Experience

Semiconductor Readiness Organization, UF Nanoscale Research Facility Sep 2024 – Present

- Fabricated MOS capacitors in the NRF cleanroom: dry oxidation, spin-coating, photolithography, HF wet etch, sputter deposition.

Skills

Languages: C, C++, Python, MATLAB, VHDL, SystemVerilog, AVR assembly
EDA & Simulation: Altium Designer, LTspice, Cadence Virtuoso, Quartus, QuestaSim (SVA, constrained-random verif.)
Embedded & Lab: NVIDIA Jetson, FLIR/GigE Vision, DMA- and interrupt-driven firmware, Linux, Git; thermal imaging, I–V characterization, oscilloscope/AWG/network analysis; cleanroom microfabrication